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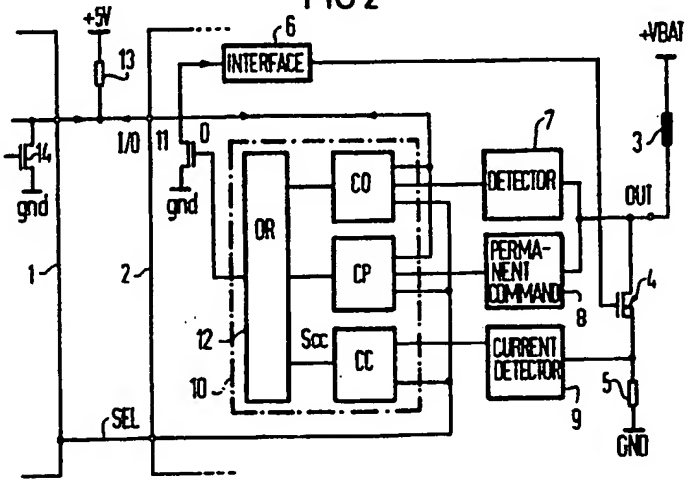
(54) Device for the detection and discrimination of functional faults in an electrical power supply circuit.

(57) The device comprises a control circuit (2) integrating a power transistor (4) controlling the electrical power supply of a load (3), detectors (7, 8, 9) and a logic circuit (10) connected to a computer (1) by two lines (I/0) and (SEL). According to the invention, the computer selectively and successively controls, by specific combinations of logic signals applied on the lines (I/0) and (SEL), several logic sub-circuits for the detection and identification of functional faults in the power supply circuit of the load (permanent control, short-circuit, open circuit), the circuit (2) in return imposing on the line (I/0) logic levels representative of the presence or absence of faults, during time intervals in which the computer is configured to read these levels.

Application to the diagnosis of the functional status of electro-valves forming part of a wheel anti-locking device on a vehicle.

FIG 2



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The present invention relates to a device for the detection and discrimination of functional faults in an electrical power supply circuit and, more particularly, to such a device adapted to a power supply circuit of a load connected in series with an electronic switch controlled by a computer.

At present, in the motor vehicle industry for example, electronic computers are used for controlling various actuators, injectors, electro-valves, ignition coils, electric motors, etc. By way of non-limitative example the electro-valves of motor vehicle wheel anti-locking devices may be quoted with respect to this. Figure 1 of the appended drawing shows schematically the electronic section of a known device of this type, controlling six electro-valves EV-0 to EV-5 used for modulating the pressure in the braking circuits of wheels, after detection of the imminence of the skidding of at least one of the wheels of the vehicle with respect to the ground. The excitation winding of each electro-valve is connected on the one hand to a voltage source +Vbat constituted by the battery of the vehicle and, on the other hand, to an OUT pin of a control circuit (CC-0 to CC-5) for the power supply of the winding by a selective connection to ground GND. In order to do this, the circuit conventionally comprises a power transistor, of the MOS type for example, whose drain-source circuit is connected between the OUT pin and the ground pin GND. The switching of the power transistor is ensured by signals coming from a main computer and supplied to the input IN of the control circuit, via an input bus. Such control circuits are well known and normally include, in addition to a power section in which the current coming from the battery flows, a section powered at low current and capable of processing logic signals used on the one hand for controlling the power transistor and on the other hand for the detection of functional faults which are signalled to the main computer by signals emitted on a "STATUS" pin and transmitted to the computer by means of a "status" bus. Such a control circuit is commonly called a "smart power circuit" —— as it is both capable of controlling an actuator using its power section and of processing logic signals, for example, for the detection of short-circuits or other faults capable of preventing the correct functioning of an electro-valve and, more generally of the whole of the device. Furthermore the anti-locking device can also comprise an auxiliary monitoring computer which executes redundant computations on the signals received by the main computer in order to check the correct functioning of the latter. A power supply voltage VCC, for example +5 volts, supplies each of the control circuits and computers and return load resistors connected to the inputs IN-0 to IN-5 of the main computer connected to the status bus and to lines interconnecting the pins 0 to 5 of the two computers in order to provide for dialogue data exchanges between them.

In the abovementioned application to the control of anti-locking of the wheels of a motor vehicle, it is very important to know the functional state of each of the electro-valves as a functional fault of one or more of them can seriously affect the safety of the driving of the vehicle. It is observed however, in the diagram of the known device shown in Figure 1, that the transmission to the computer of data generated by the control circuits CC-0 to CC-5, relating to possible functional faults in the circuits or in the electro-valves associated with them, requires that a rather large number of input and output pins (or "ports") are available on the computers. In addition to six output pins OUT-0 to OUT-5, used for sending to each control circuit commands for switching power transistors, each computer must comprise input pins IN-0 to IN-5 in order to receive data relating to possible functional faults in the control circuits. Unfortunately, the microprocessors currently available for equipping devices of the type shown in Figure 1 comprise a limited number of input-output pins while it is desired to increase the number of actuators capable of being controlled by one microprocessor. It therefore appears that this increase can only be made possible by a reduction in the number of lines used for exchanging data between each control circuit and the associated computers, while retaining all the functions mentioned above.

Furthermore, the known control circuits, after detection of a functional fault (thermal overload, short-circuit load, open circuit load etc...) are limited to maintaining the STATUS line at logic 0, a measure which does not allow the computer to determine the nature of the fault. This is a substantial disadvantage as all of the functional faults are not equally important and it would be useful for the functioning in degraded mode of the control device, established by the computer on receiving a fault signal, to be able to take account both of the nature of the fault and of the position of the electro-valve which is affected by it. By way of example, a permanent control or excitation of an electrovalve due to an internal or external short-circuit of the power transistor of the control circuit associated with this electro-valve can give rise to a drop in pressure in the hydraulic circuit controlling a wheel brake, which dangerously affects the driver's ability to stop his vehicle. The degraded functioning established by the computer should be able to take account of the dangerous nature of such a failure, in order still to ensure the safety of the braking.

The object of the present invention is therefore to produce a device for the detection of functional faults in an electrical power supply circuit of a load, in which the number of wire links between a control circuit of this power supply and a computer programmed to emit control signals for the power supply of the load, and to organize the detection of possible functional faults of this power supply, is substantially reduced with

respect to the number of links currently used in the known devices of the same type.

Another object of the present invention is produce such a device allowing the discrimination of the faults signalled to the computer as a function of their nature.

Another object of the present invention is to produce such a device allowing the provision of a periodic diagnostic test of the functional status of the device, in real time, the time interval dedicated to this diagnostic test being very short in order not to disturb the functioning of the loads.

Another object of the present invention is to produce such a device allowing the installation of an auxiliary computer for monitoring the main computer.

Another object of the present invention is to produce such a device allowing, in the case of the control of the power supply of several different loads, detection of possible cross-talk occurrences having origins which are internal or external to the control circuits, by the implementation of specific software means in the computer.

These objects of the invention are achieved with a device for the detection and the discrimination of functional faults in at least one electrical power supply circuit for a load placed in series with an electronic switch of which one control pin is connected to a computer by a control line transmitting to that pin switching signals controlled by the computer, this device comprising means of detection of at least one functional fault from the group formed by: the short-circuit of the load, the permanent control of the load and the opening of the power supply circuit of that load, characterized in that these means of detection comprise at least one detector sensitive to an electrical characteristic of a predetermined point in the power supply circuit of the load and capable of forming a logic signal representative of the position of the value of this characteristic with respect to a predetermined value, and a logic circuit connected to the output of the detector, to the control line and to a selection line both connected to the computer in order to transmit to the logic circuit at least one combination of logic signals emitted by the computer and capable of activating this circuit for the purpose of the detection of a possible presence of a particular fault and for the production of a signal representative of the detected situation, the output of the logic circuit then controlling means of imposition, on the control line, of one of two logic states respectively corresponding to the presence or the absence of the fault, the computer comprising means for configuring in readout mode that one of its ports which is connected to the control line when the logic state of the latter is imposed by the logic circuit and of identifying a possible fault by the readout of this state.

The logic circuit comprises several sub-circuits each connected to one of the said detectors, the computer comprising means for establishing, on each of the control and selection lines, a plurality of series of logic levels according to line-to-line combinations each capable of activating one of the sub-circuits, the sub-circuits reacting successively to the reception, when they are activated, of a signal coming from an associated detector in order to impose on the control line a logic state corresponding to the received signal while the computer is reconfigured in order to read the state of this line, the series of logic states thus imposed on the control line by the various sub-circuits being identified by the computer as representative of the presence or absence of a particular fault.

In the appended drawing given by way of example only:

Figure 1 is a block diagram of the device for the detection of functional faults of several electrical power supply circuits of loads described in the preamble of the present description,

Figure 2 is a functional block diagram of a control circuit incorporated in the device for the detection and discrimination of functional faults according to the invention,

Figure 3 shows several timing diagrams for the logic states established on two pins of the circuit of Figure 2, for the detection of several different functional faults and the discrimination of these faults,

Figure 4 is a timing diagram of various logic state sequences established on a control line connecting the control circuit of Figure 2 to the computer, depending on whether the controlled power supply circuit is in a normal functional state, in a short-circuit state, in an open circuit state or in a permanent control of the load state,

Figure 5 is a block diagram of a preferred embodiment of the control circuit of Figure 2, in particular of its logic section, and

Figure 6 is a block diagram of the device according to the invention, adapted to the control of the electrical power supply of several loads by means of as many circuits of the type shown in Figures 2 and 5, controlled by a main computer monitored by an auxiliary computer.

Reference is made to the block diagram of Figure 2 and to the timing diagram of Figure 3 in order to describe the structure and the functioning of the device for the detection and discrimination of functional faults according to the invention.

Figure 2 shows a computer 1 connected by a control line I/0 and by a "selection" line SEL to a control circuit 2 for the electrical power supply of a load 3 connected between an electrical energy source +Vbat

and an "OUT" pin of the the circuit 2 connected to the drain of a power transistor 4 of the N-MOS type for example, whose source is connected to ground via a measuring resistor 5 whose presence will be justified below. An interface circuit 6 is interposed between the I/0 line and the control electrode of the transistor 4 in order to adapt logic signals received from the computer via the I/0 line to the control of the switching of this transistor. The circuit 2 furthermore comprises an excess voltage detector 7, a permanent control detector 8, a current detector 9 and a logic circuit 10 fed by the signals supplied by these detectors in order to control means of imposition of a logic state on the line 11, such as a current source 11 connected between the pin of the circuit 2 which is connected to the I/0 line and ground GND.

Thus, the control circuit 2 is the type of circuit known by the name "intelligent power circuits" comprising a power section (the transistor 4) and a low current logic section associated with detectors, the assembly being integrated on the same silicon chip in order to be installed between a computer and a load whose power supply is controlled by the signals generated by the computer. In the non-limitative application to the control of a wheel anti-locking device mentioned above, the device can comprise several identical control circuits each associated with a load constituted by the winding of an electro-valve controlling the pressure of a braking fluid in a wheel brake.

The logic section essentially comprises three sub-circuits CO, CP, CC fed by signals coming from the detectors 7, 8 and 9 respectively. As will be seen below, the sub-circuits CO, CP and CC are designed to respectively ensure the detection of an opening of the power supply circuit of the load, of a permanent control of that load, and of a short-circuit of the said load. The outputs of the sub-circuits CO, CP, CC, are connected to an OR gate 12 whose output controls the activation of the current source 11 in order to take the I/0 line to a "low" logic level when there is detection of a short-circuit or of a permanent control. The detection of an open circuit results in the imposing of a "high" logic level on the I/0 line.

According to the present invention, the selection line SEL, whose function will be described in detail below, which connects a pin of the computer 1 to a corresponding pin of the circuit 2, is also connected to an input of each of the sub-circuits CO, CP, and CC. The I/0 line which connects another pin of the computer to a corresponding pin of the circuit 2, is connected to an input of the circuit CO and to an input of the circuit CP, these two circuits thus having three inputs while the circuit CC has only two.

If the circuit of Figure 2 is compared with one of the circuits CC-0 to CC-5 of the known device in Figure 1, it can be seen that these circuits are all connected by two wires to the computer. However, when the device according to the invention includes more than one load to be controlled, and therefore more than one control circuit such as 2, the SEL line is common to all of the control circuits, as will be seen later in connection with the description of Figure 6, which allows, according to an advantageous characteristic of the present invention, a substantial saving to be achieved in the number of wire links to be established between the computer and the control circuit.

As will also be seen below, the present invention is based on the emission, by the computer, of a sequence of specific combinations of logic signals on the I/0 and SEL lines in order successively to command the interrogation of the sub-circuits CO, CP and CC, this interrogation sequence provoking in return the establishment by the logic circuit 10 of a sequence of logic states on the I/0 line, which is then bidirectional, this sequence being read by the computer 1 in order to determine not only the existence of a fault on a certain controlled load but also, according to another advantageous characteristic of the present invention which does not depend on the number of control circuits incorporated in the device, the nature of the detected fault on a certain load. The computer can therefore be programmed in such a way as to establish a functioning in degraded mode of the control of the power supply of the loads, adapted to the nature of the faults detected in these loads. In an application such as that mentioned above by way of example to the control of a wheel anti-locking device of a vehicle, such an application allows the braking safety of that vehicle to be improved.

It will be noted that the use of two wires for commanding the interrogation of a logic sub-circuit allows the initiation of the interrogation of four sub-circuits by the four possible combinations of logic states on these lines. Associated with a sequential interrogation of the sub-circuits, this capability allows the differentiation of the fault signals, according to their nature, even if these fault signals were of four different types. In fact, for the control of the electrical power supply of a load, it is appropriate to identify three functional faults only: the short-circuit of the load, the opening of the power supply circuit of the load and the permanent control of the load resulting from an internal short-circuit of the transistor 4 or from an external short-circuit of this transistor 4 by the grounding of the wire normally connecting the load to an "OUT" pin of the circuit 2, connected to the drain of the transistor 4.

Reference is now made to the timing diagrams shown in Figure 3 in order to describe in greater detail the combinations of logic states and transitions established by the computer on the I/0 and SEL lines, in order to initiate the interrogation of the various sub-circuits CC, CO, and CP.

Thus, at an instant t_1, the computer takes the SEL line to the logic 1 state. The logic function executed by the sub-circuit CC is then such that if the current detector sends to the circuit CC a logic signal signifying an excess current read by the intermediary of a voltage reading at the terminals of the measuring resistor 5, this excess current resulting from a short-circuit of the load, the output of the logic sub-circuit goes to the 1 state in order to command the putting of the current source 11 into the conducting state, which establishes the logic 0 state on the I/0 line while the computer has configured its port connected to this line in the input mode, in order to read the logic state imposed on this line by the logic circuit 10.

It is necessary to pause for a moment on the functioning of the I/0 line which, according to the invention, is bidirectional since it allows, on the one hand, the computer to send control signals for switching the transistor 4, via the interface 6, and interrogation signals to the sub-circuits CO and CP, and on the other hand, the transmission of logic signals to the computer, which are representative of the responses generated by the sub-circuits CC, CO and CP subsequert to the sequential interrogations of these circuits by the computer. In this respect the presence of a pull-up load 13 connected between a power supply source of the device, for example a +5 volts source, and the I/0 line, between the corresponding pins of the computer and the circuit 2 will be noted. Conventionally the computer comprises a transistor 14, of the MOS type for example, which allows the controlling of the state of the I/0 line. Thus the pull-up load 13, the transistor 14 and the current source 11 provide the function known as the "hard-wired OR" function which allows either the current source 11 or the transistor 14 to draw the I/0 line to the low state.

Reference is again made to the timing diagram of Figure 3, and more particularly to the one concerning the status of the SEL and I/0 lines for the control of the detection of a possible short-circuit of the load, in order to note that if the I/0 line is not in the logic 1 state prior to the instant t_1 (curve in broken line), the computer commands the changing of this line to the 1 state in order to thus command the conduction of the power transistor 4 and to allow the detection of a possible short-circuit situation. If therefore, as has been seen above, such a short-circuit situation exists, the I/0 line is taken to the low state after a time interval (t_1, t'_1) due to internal time constants of the current detector 9. After this instant t'_1 the input port of the computer 1 connected to the I/0 line is reconfigured in the input mode by the computer and the low state established on this line by the putting into conduction of the current source 11 commanded by the logic circuit 10 is therefore read by the computer which is thus informed of the presence of a short-circuit in the power supply circuit of the load 3. If, on the other hand, no short-circuit is detected, the I/0 line is maintained, after the instant t'_1, by the source 11 in the high logic state and the re-reading of this line by the input port of the computer allows the latter to be informed of the absence of short-circuit and therefore of a normal situation from this point of view.

For the self-protection of the control circuit in the case of a short-circuit of the load, the sub-circuit CC comprises a short-circuit memory flip-flop, as will be seen later in connection with the description of the embodiment of the circuit shown in Figure 5. It is therefore necessary to provide in the sub-circuit CC means for resetting this flip-flop to zero at the instant t_1. These means are controlled by the changing to the high level of the SEL line controlled by the computer to interrogate the sub-circuit CC, as will be seen later again in connection with the description of the embodiment in Figure 5.

The description will now be given of the means used for providing a detection of an accidental opening of the power supply circuit of the line. The message of activation of the sub-circuit CO then emitted by the computer is constituted by the changing to the high state of the SEL line, if the latter was not already in that state, at an instant t_2 later than the short-circuit detection phase described above, the computer commanding at this instant t_2 a transition to the low state of the I/0 line which causes the cutting off of the power transistor 4. In the absence of accidental opening of the power supply circuit of the load 3, this sudden breaking of this circuit by the cutting off of the transistor 4 must normally cause the appearance of a high transient excess voltage on the OUT pin of the circuit 2, constituting the common point between the load 3 and the drain of the transistor 4, if this load exhibits inductance. In the presence of an excess voltage, i.e. in normal operation, the excess voltage detector 7 transmits a signal to the sub-circuit CO and this sub-circuit processes this signal in such a way as to transmit to the OR gate 12 a high state signal which draws the I/0 line to a low state. In the absence of the detection of such excess voltage, the sub-circuit CO causes, on the contrary, the drawing of the I/0 line to the high state by the cutting off of the current source 11. This cutting off occurs after a time interval (t_2, t'_2). After t'_2 the computer has reconfigured its port connected to the I/0 line to the input mode in order to re-read, on the I/0 line, either a high state signifying the existence of an open circuit or a low state signifying the absence of an accidental opening of the circuit. Obviously, the detection of excess voltage carried out for the revealing of a nonopening of the power supply circuit of the load 3 can only be considered if the latter has an excess voltage-generating inductive component at the breaking of the power supply circuit, as is the case with loads allowing the control of numerous actuators such as electromagnets or electro-valves. If the load to be controlled does not have such an inductive

component, the detection of an accidental opening of the circuit should of course make use of other means of revelation, the choice of these means as a function of the characteristics of the load being within the normal field of knowledge of those skilled in the art.

The description will now deal with the means used in the invention for ensuring the detection of a state of permanent control of the load, resulting from a short-circuit of the power transistor 4, which short-circuit may be internal to the control circuit 2 or external to the latter, when the line which connects the load 3 to the OUT pin of the circuit accidentally comes into contact with ground. The interrogation message addressed by the computer to the sub-circuit CP is then constituted as follows. On the one hand the SEL line, which was maintained in the high state during the short-circuit and open-circuit detection phases, is then taken, at an instant t_3 later than the open circuit detection phase described above, to the low state. Simultaneously, the I/O line is forced to the low state by the computer even if the latter were already previously in this state because of a previous control of the current source 11 to that effect. The forcing to the low state of the I/O line causes the cutting off of the MOS transistor 4 which normally should cause, as seen above in connection with the detection of a possible accidental opening of the circuit, an excess voltage on the OUT pin. If the load is permanently controlled, the transistor 4 therefore being short-circuited, such an excess voltage would obviously not appear and, on the contrary, the voltage on the OUT pin must be close to zero. The permanent control detector 8 is therefore constituted by a comparator which, in the case in which the voltage on the OUT pin is greater than a predetermined value close to 0, sends a signal to the sub-circuit CP which transmits a logic 1 state signal to the OR gate 12 in order that the latter forces the I/O line to the low state, while the input port of the computer 1 connected to this line is reconfigured in the input mode starting from an instant t'_3 later than instant t_3. If on the contrary the computer reads, after the instant t'_3, that the I/O line is in the logic 1 state, the information is understood by the computer as representing a normal state of the power supply circuit of the load, at least as regards the permanent control of that load.

The sequence of interrogation of the sub-circuits CC, CO, CP, has been described above in that order but the invention of course is not limited to such a sequence and its various phases could be placed in a different order. However, the order described above is preferred as it allows, by holding the SEL line at the same high level during the consecutive phases associated with the detection of a short-circuit and of an open circuit, the limitation of the number of edges on the SEL line which avoids too many switchings of the power transistor in the case of a permanent short-circuit. The chosen sequence also ensures a minimum number of switchings of the power transistor into the cut-off state, in order to avoid a heating up of the transistor under the effect of the excess "clamp" voltages (to use the English term) during the diagnostic sequence for possible failures in the electrical power supply of each load.

The three sequential tests described above allow the following sequences of states read by the computer to be defined.

Logic state sequence	Faults detected	Circuit status
0 0 0	$CC + \overline{CO} + CP$	Permanent SHORT-CIRCUIT
0 0 1	$CC + \overline{CO} + \overline{CP}$	Impossible (CC = 0 implies CP = 0)
0 1 0	$CC + CO + CP$	Impossible (CC = 0 implies CO = 0)
0 1 1	$CC + CO + \overline{CP}$	Impossible (CC = 0 implies CO = 0, CP = 0)
1 0 0	$\overline{CC} + \overline{CO} + CP$	CP transient during the test
1 0 1	$\overline{CC} + \overline{CO} + \overline{CP}$	NORMAL functioning
1 1 0	$\overline{CC} + CO + CP$	PERMANENT control
1 1 1	$\overline{CC} + CO\,\overline{CP}$	OPEN CIRCUIT

In the above table, the presence of a short-circuit, an open circuit or a permanent control is represented by CC, CO and CP respectively, the complementing of these symbols representing the absence of the fault.

After filtering by software provided for this purpose and installed in the computer, over several test cycles, it appears that the logic state sequences corresponding to the principal faults are as follows:

Sequence	Status of the circuit
101	NORMAL FUNCTIONING
000	SHORT-CIRCUIT
111	OPEN CIRCUIT
110	PERMANENT CONTROL

Reference is now made to Figure 4 of the appended drawing which shows the timing diagrams of the signals present on the I/0 line connecting the computer to a control circuit of the device according to the invention, during the load test phases, for the various cases of faults.

In the various timing diagrams of the states of the I/0 line it will be noted that the 0 levels imposed on re-reading by the control circuit are shown slightly shifted above the 0 levels imposed on the line by the computer in order to allow it to be more easily to distinguished whether it is the computer or the control circuit which is acting on this bidirectional line.

Figure 4 also shows the timing diagram of the logic states of the selection line SEL which allows the various test phases performed to be distinguished.

At this point in the description of the device according to the invention it should be noted that, in the application to a wheel anti-locking device mentioned above by way of example, the computer periodically computes the state, conducting or cut-off, in which each electro-valve of the anti-locking device should be in order to ensure braking without skidding of the vehicle when the imminence of such skidding is detected. This computation is carried out simultaneously for all of the electro-valves, numbering six for example, a very large number of times per second, for example every five milliseconds.

According to the invention, the test sequence described above is therefore carried out at the beginning of each five millisecond period which separates two possible corrections by the computer of the state of the electrovalves. It is important that this test sequence should be very short in order that the switchings of the I/0 line which it involves do not disturb the functioning of the electro-valves. For this purpose, according to the invention, the three short-circuit, open circuit and permanent control tests are carried out in 50 microseconds each, each test being sub-divided into a period of 20 microseconds during which the computer controls the I/0 line and a following period of 30 microseconds during which the port of the computer which is connected to that line is configured in the input mode to allow the reading by the computer of the states imposed on the I/0 line by the associated control circuit. Thus all of the tests are carried out in 150 microseconds, simultaneously on all of the electro-valves, this taking place every 5 milliseconds, which ensures a real-time detection of faults which possibly appear, without this detection disturbing the control of the electro-valves by the computer.

The invention is not limited to the parallel test procedure on all of the loads described above and could of course use a series test procedure of the said loads, as is well known. In the series test procedure, the sequence of tests is applied successively to each load. This method has the disadvantage of giving the computer an image of all the functioning conditions of the said loads only once all of the interrogated loads, for example for six loads, are at the end of six cycles of 5 milliseconds, i.e. 30 milliseconds, if the application example described above is taken again. In comparison, the parallel test procedure allows this image to be obtained every 5 milliseconds. On the other hand the series test procedure has the advantage over the parallel test procedure of allowing a very simple implementation of cross-talk tests because each electrovalve is separately interrogated by the computer.

In fact, in the case in which the device according to the invention is used in a system requiring the control of several loads, as is the case in the wheel anti-locking device mentioned above which has 6 electro-valves and therefore 6 loads, it can be advantageous to add to the test sequence described above a cross-talk test in order to diagnose possible interactions and short-circuits between the inputs and the outputs of the control circuits (so called "internal" cross-talk) or the between the wires connecting the loads to their respective control circuits (so called "external" cross-talk).

Cross-talk occurrences such as these can be diagnosed by successive test cycles during each of which only one load is excited by the computer, during the permanent control test. The status sequences taken either during writing or during reading during the permanent control test are analysed by software loaded in the computer which, by noting small differences between the timing diagrams taken on the I/0 lines, can identify the control circuits subject to cross-talk of internal or external origin.

Reference is now made to Figure 5 of the appended drawing which shows in detail the logic section of a control circuit incorporated in the device according to the invention, a block diagram of the principle of which is shown in Figure 2. The various blocks in Figure 2 are marked by broken lines in the block diagram

of Figure 5 and have been given the same references. Only the features of the circuit in Figure 5 which have not been described in connection with the examination of Figure 2 will be described below.

The logic section of the circuit is produced using NOR, NAND and NOT complementary logic gates (these terms being the commonly used English terms for denoting these gates). Thus, the OR function of the circuit in Figure 2 is achieved by means of a NOR gate 13 and an inverting NOT 14, connected between the output of the NOR gate 13 and the current source 11, conventionally produced by means of a current mirror circuit.

The voltage detector 7 is activated following the breakdown of a Zener diode 15 which is reverse connected between the OUT pin of the control circuit and this detector, during the formation of an excess voltage on this pin following the cutting-off of the power transistor 4 by a signal emitted by the computer on the I/0 pin of the circuit and transmitted by the interface circuit 6. The output signal of the detector 7 is stored in a conventional flip-flop formed from two NAND gates 16 and 17. The sub-circuit CO is thus constituted by this flip-flop and a NOR gate 18 having two inputs respectively connected to the I/0 pin of the circuit and to the output of the flip-flop (16, 17), the gate 17 of the flip-flop comprising an input connected to the SEL line, the sub-circuit thus being fed with signals coming from the detector 7 and from the SEL and I/0 lines in order to function as described with reference to Figure 2.

Incidentally, the presence of a diode 18 will be noted between the terminal common to the Zener diode 15 and the input of the detector 7 on the one hand, and the gate of the transistor 4 on the other hand, for protecting the latter by cutting off on breakdown of the diode 15 on the appearance of an excess voltage on the OUT pin of the circuit. A ground resistor 19 allows the detector 7 to measure the excess voltage.

The sub-circuit CP is constituted by a simple NOR gate 20 having three inputs respectively connected to the I/0 pin of the circuit, to the SEL line and to the output of a detector for detecting an internal or external short-circuit of the power transistor 4, this short-circuit causing a permanent control of the load connected to the OUT pin of the circuit. The output of the NOR gate 20 is connected to an input of the NOR gate 13. As has been seen above the detector 8 is constituted by a simple voltage comparator supplied with a reference voltage close to zero, of 1 or 2 volts for example. A return load resistor 21 is connected to the input of the detector. A diode 22 is reverse connected between the OUT pin of the circuit and the point common to the return load and to the input of the detector 7. The diode D22 avoids the return of the high voltage (55V approximately during the "CLAMP" period) of the OUT output to the internal power supply voltage VCC via the resistor 21.

In the case of an open circuit of the load, the OUT output tends to remain at a potential close to 0 V since this output becomes floating. It is therefore necessary to fix this potential at a level such that it is possible to disassociate the open circuit fault CO from the permanent control fault CP (this fault being detected, as seen above, by the presence of a low voltage on this OUT output). The function of the resistor 21 is therefore to maintain a potential close to that of the supply in the case of an open circuit.

The sub-circuit CC essentially comprises a flip-flop comprising two NAND gates 23 and 24 for storing an excess current signal emitted by the detector 9, and a detector of rising edges on the SEL line constituted from a flip-flop having two NAND gates 25 and 26, one input of which is connected to this SEL line, and from a NAND gate 27 having two inputs respectively connected to an output of the flip-flop (25, 26) and to the SEL line in order to transmit on its output a signal for resetting the flip-flop (23, 24) to zero when a rising edge is detected on the SEL line. The output of the gate 23 of the flip-flop (23, 24) is connected to an input of the NOR gate 13.

It will also be noted that the interface 6 is conventionally constituted by a voltage multiplier 28 necessary for the control of the gate of the power transistor 4, this multiplier itself being supplied by a voltage source VCC for the power supply of the control circuit 2 and of the computer associated with it. In this interface there is a NAND gate 29 having two inputs connected to the I/0 pin and to the output of the NOR gate 13. The output of the NAND gate 29 controls an inhibit input 30 of the voltage multiplier 26 and the gate of an MOS transistor 31 controlling the discharging to ground of the gate of the transistor 4. In the case of a holding of the I/0 line at the logic "1 level (caused for example by an accidental short-circuit of the latter to +VCC), it is necessary to be able to ensure the cutting of the power transistor during the presence of a short-circuit in the load. The NAND logic gate 29 carries out this safety function preventing the destruction of the power switch. Furthermore, the voltage multiplier 26 necessary for the control of the gate of the power transistor, consumes a non-negligible current from the VCC power supply. It is therefore preferable to provide an inhibit input on this multiplier in order to reduce the consumption of the logic circuit when the latter is not controlling the load.

Transistors 32, 33 are connected as resistors between the I/0 and SEL lines respectively and ground in order to reference the potentials of these pins in case the latter become disconnected, this conforming with the so-called "FMECA" method of analysis of electrical failure in a system.

All of the components shown in Figure 5 can be integrated on one chip in a package having five pins: VCC, I/0, SEL, OUT and GND, such as a so-called "Pentawatt" TO 220 package. Because, according to the invention, the SEL line is common to several control circuits it appears possible to have two control circuits according to the invention on the same chip in a TO 220 type package for example having seven pins and called a "Heptawatt" package: VCC, GND, two I/0 pins, two OUT pins, and a SEL pin. The size of the device according to the invention can thus be reduced while lowering its manufacturing cost.

Throughout the above description the control circuits used are connected to the "ground" side of the load to be controlled. It is clear that the invention is not limited to such an arrangement and that it obviously extends to devices in which the control circuits are connected to the power supply circuit of load, on the side where the power supply source of this circuit is located, as is frequently the case.

Figure 6 of the appended drawing shows the device according to the invention, integrated with a control device for six loads comprising, in order to establish a comparison with the (known) device of Figure 1, a main computer and an auxiliary monitoring computer and six control circuits 2-0 to 2-5 according to that described in Figure 5. Superficially, the device thus has the same configuration as that of Figure 1 but it is immediately apparent that as the SEL line is common to all of the circuits and connected to a single OUT pin of the main computer, the control of the circuits 2-0 to 2-5 by the computer here uses only seven pins of the latter instead of twelve (IN-0 to IN-5 and OUT-0 to OUT-5) on the computer of the device in Figure 1. Similarly, the monitoring computer dedicates no more than six pins instead of twelve to the monitoring of the main computer. This results in a reduction in the same proportion in the wire connections between the computers and the control circuits which is an essential advantage obtained by the present invention. As seen above, another no less essential advantage provided by the invention is that it allows the discrimination of the sought faults in order to improve the degraded mode functioning of the control of the power supply of the loads.

The invention is of course not limited to the embodiment described and shown which has been given only by way of example, nor to the application mentioned above to the control of the electro-valves of a wheel anti-locking device of a vehicle. On the contrary it extends to the control of the electrical power supply of any load, isolated or in a group of such loads, controlled by "intelligent" or other power circuits.

Neither is the invention limited to the detection and discrimination of four functional faults at most. The use of an additional selection line would allow the maximum number of detectable faults to be increased to 9 for example.

Furthermore the invention is not limited to a device produced in MOS technology, this device being able to call upon any current technology for producing integrated circuits, for example the TTL technology.

Claims

1. Device for the detection and the discrimination of functional faults in at least one electrical power supply circuit for a load placed in series with an electronic switch of which one control pin is connected to a computer by a control line (I/0) transmitting to that pin switching signals controlled by the computer, this device comprising means of detection of at least one functional fault from the group formed by: the short-circuit of the load, the permanent control of the load and the opening of the power supply circuit of that load, characterized in that these means of detection comprise at least one detector (7 ; 8 ; 9) sensitive to an electrical characteristic of a predetermined point in the power supply circuit of the load and capable of forming a logic signal representative of the position of the value of this characteristic with respect to a predetermined value, and a logic circuit (10) connected to the output of the detector (7 ; 8 ; 9) , to the control line (I/0) and to a selection line (SEL) both connected to the computer (1) in order to transmit to the logic circuit at least one combination of logic signals emitted by the computer and capable of activating this circuit for the purpose of the detection of a possible presence of a particular fault and for the production of a signal representative of the detected situation, the output of the logic circuit (10) then controlling means of imposition, on the control line (I/0), of one of two logic states respectively corresponding to the presence or the absence of the fault, the computer (1) comprising means for configuring in readout mode that one of its ports which is connected to the control line (I/0) when the logic state of the latter is imposed by the logic circuit and of identifying a possible fault by the readout of this state.

2. Device according to Claim 1, characterized in that the logic circuit comprises several sub-circuits (CO, CP, CC) each connected to one of the said detectors (7, 8, 9), and in that the computer (1) comprises means for establishing, on each of the lines (I/0) and (SEL), a plurality of series of logic levels according to line-to-line combinations each capable of activating one of the sub-circuits (CO, CP, CC), the sub-circuits reacting successively to the reception, when they are activated, of a signal coming from an associated

detector in order to impose on the line (I/0) a logic state corresponding to the received signal while the computer is reconfigured in order to read the state of this line, the series of logic states thus imposed on the line (I/0) by the various sub-circuits being identified by the computer as representative of the presence or absence of a particular fault.

3. Device according to Claim 2, in which the electronic switch is a transistor (4), characterized in that one (9) of the detectors is sensitive to the presence of an excess current in the circuit controlled by the transistor (4) such that it transmits a logic signal to a sub-circuit (CC) activated by a predetermined logic level established on the line (SEL) by the computer, the sub-circuit then controlling the said means of imposition (11) such that the latter impose on the line (I/0) a predetermined logic level representative of the presence of this excess current while the computer is configured to read the status of this line and to combine this status with the statuses imposed sequentially on the line by the other sub-circuits, in order to derive from this the possible presence of a short-circuit in the load.

4. Device according to Claim 3, characterized in that the sub-circuit (CC) comprises a flip-flop (23, 24) for storing the signal supplied by the detector (9) and a flip-flop (25, 26) for resetting the storage flip-flop to zero, controlled by a transition of the signal imposed on the line (SEL) by the computer.

5. Device according to Claim 2, in which the electronic switch is a transistor (4) connected in series with the load, on the "ground" side of the power supply circuit of the load, characterized in that one (8) of the detectors is sensitive to the voltage existing at the point of the power supply circuit common to the load (3) and to the transistor (4) in order to transmit a logic signal to a sub-circuit (CP) activated by a predetermined logic signal established on the line (SEL) and by another logic signal established on the line (I/0) capable of ensuring the cutting off of the transistor, the logic signal then emitted by the sub-circuit (CP) to the means of imposition (11) commanding the establishment on the line (I/0) of a logic level read by the computer and combined by the latter with the levels sequentially imposed on the line by the other sub-circuits and to derive from this the possible presence of a permanent control of the load.

6. Device according to Claim 5, adapted to an inductive load, characterized in that one (7) of the detectors is sensitive to an excess voltage appearing at the point of the power supply circuit of the inductive load which is common to the latter and to the transistor (4), in order to then transmit a logic signal to a sub-circuit (CO) activated by the computer by means of a predetermined logic signal established on the line (SEL) and of another logic signal established on the line I/0 and capable of commanding the cutting off of the transistor (4), the logic signal then emitted by the sub-circuit (CO) to the means of imposition (11) commanding the establishment on the line (I/0) of a logic level read by the computer and combined by the latter with the levels sequentially imposed on that line (I/0) by the other sub-circuits in order to derive from this the possible presence of an accidental opening of the power supply circuit of the load.

7. Device according to any of the previous claims, characterized in that the means of imposition (11) are constituted by a current source connected between the line (I/0) and ground and controlled by the output of the logic circuit (10).

8. Device according to Claim 7, characterised in that the computer (1) comprises a means (14) of controlling the level of the line (I/0) and in that a return load (13) is connected between a power supply source of the logic circuit and the line (I/0), between the computer and the current source.

9. Device according to any of the previous claims, adapted to a system comprising several power supply circuits for an equal number of loads, controlled by a single computer periodically correcting the state of all of the switches, characterized in that the sequence of detection of faults controlled by the computer has a short duration with respect to the periodicity of the corrections of the states of the switches.

10. Device according to Claim 9, characterized in that the computer comprises means of detection of crosstalk on the controls of the loads by processing the logic levels imposed and read on the line (I/0) by the computer.

11. Device according to any of the previous claims, characterized in that the transistor (4), the detectors (7, 8, 9), the logic circuit (10) and the associated means of imposition (11) for the control of each load are integrated in the form of a control circuit (2).

12. Device according to Claim 11, characterized in that the transistor (4) is a power transistor of the MOS type and in that the control circuit (2) then takes the form of an intelligent power circuit.

13. Device according to Claim 9, characterized in that the selection lines (SEL) associated with the loads are connected to a single pin of the computer (1).

FIG1
PRIOR ART

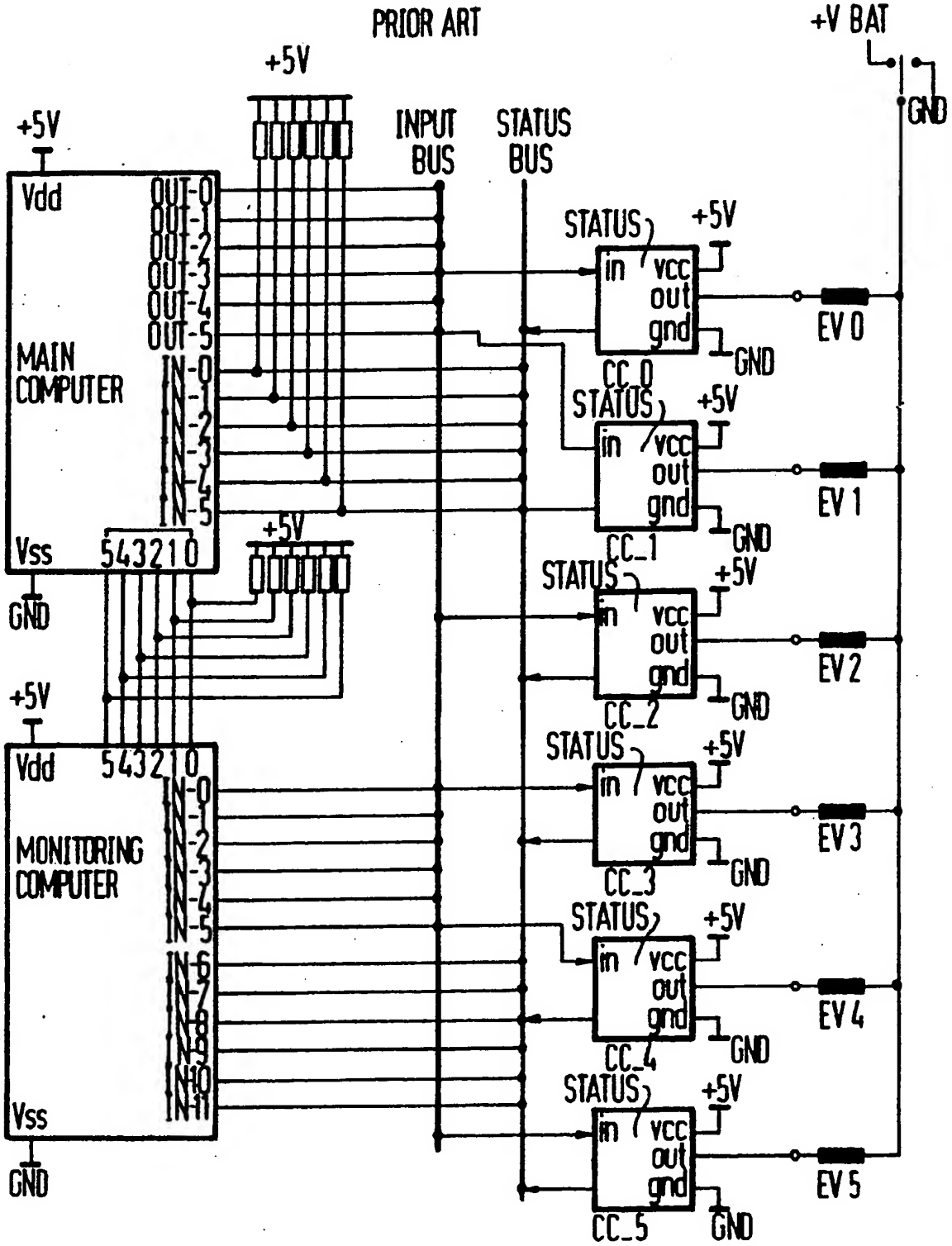


FIG 2

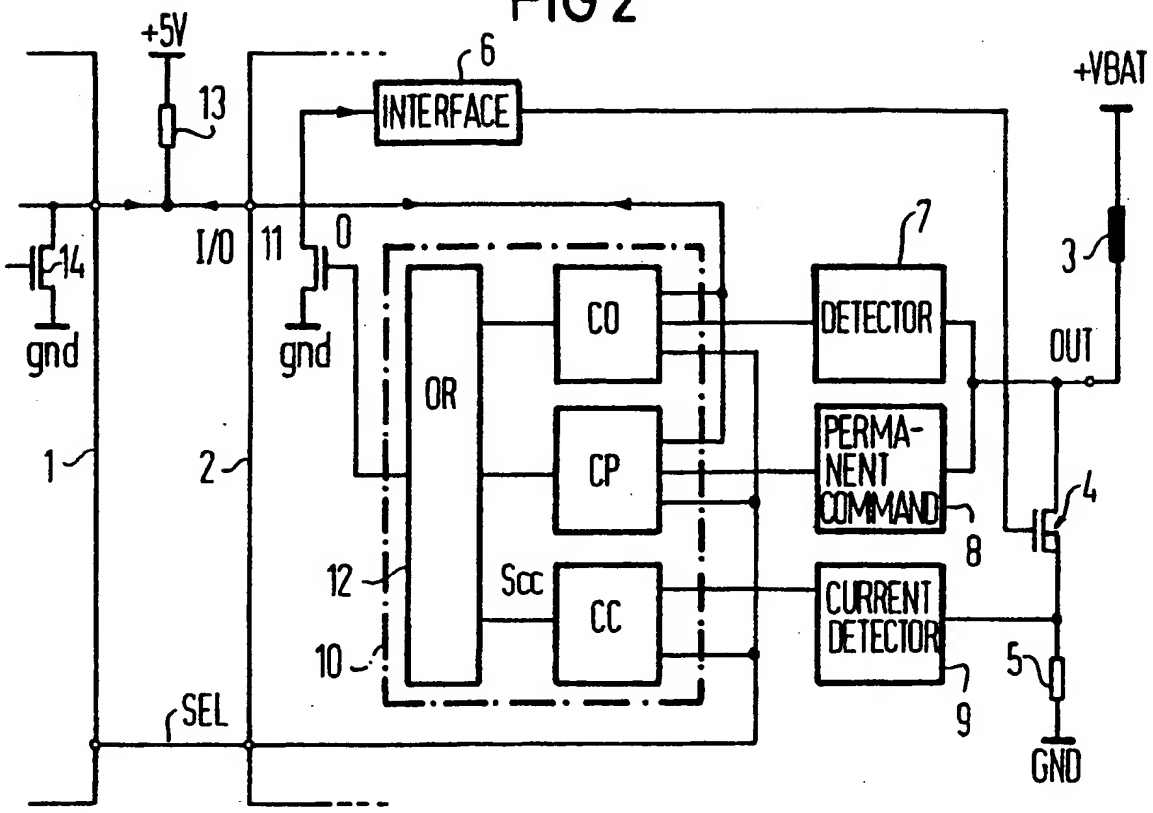
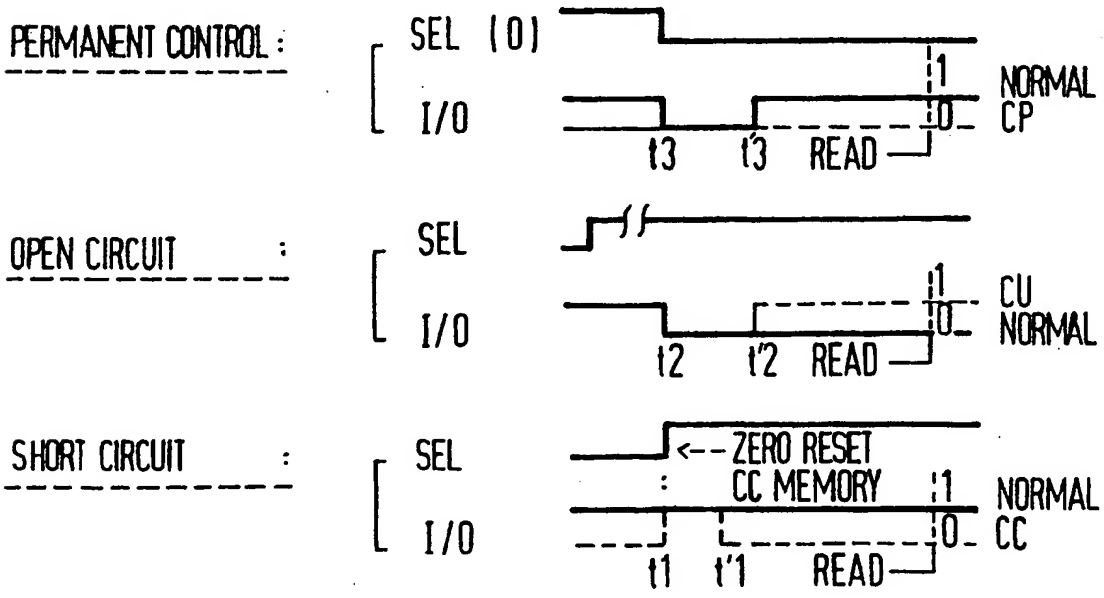

+5V
13
6
INTERFACE
+VBAT
14
I/O
11
0
7
3
gnd
gnd
OR
CO
DETECTOR
OUT
1
2
CP
PERMA-
NENT
COMMAND
4
8
12
Scc
CC
CURRENT
DETECTOR
10
5
SEL
9
GND

FIG 3


PERMANENT CONTROL :
SEL (0)
I/O
1
0
NORMAL
CP
t3
t'3
READ
OPEN CIRCUIT :
SEL
I/O
1
0
CU
NORMAL
t2
t'2
READ
SHORT CIRCUIT :
SEL
ZERO RESET
CC MEMORY
I/O
1
0
NORMAL
CC
t1
t'1
READ

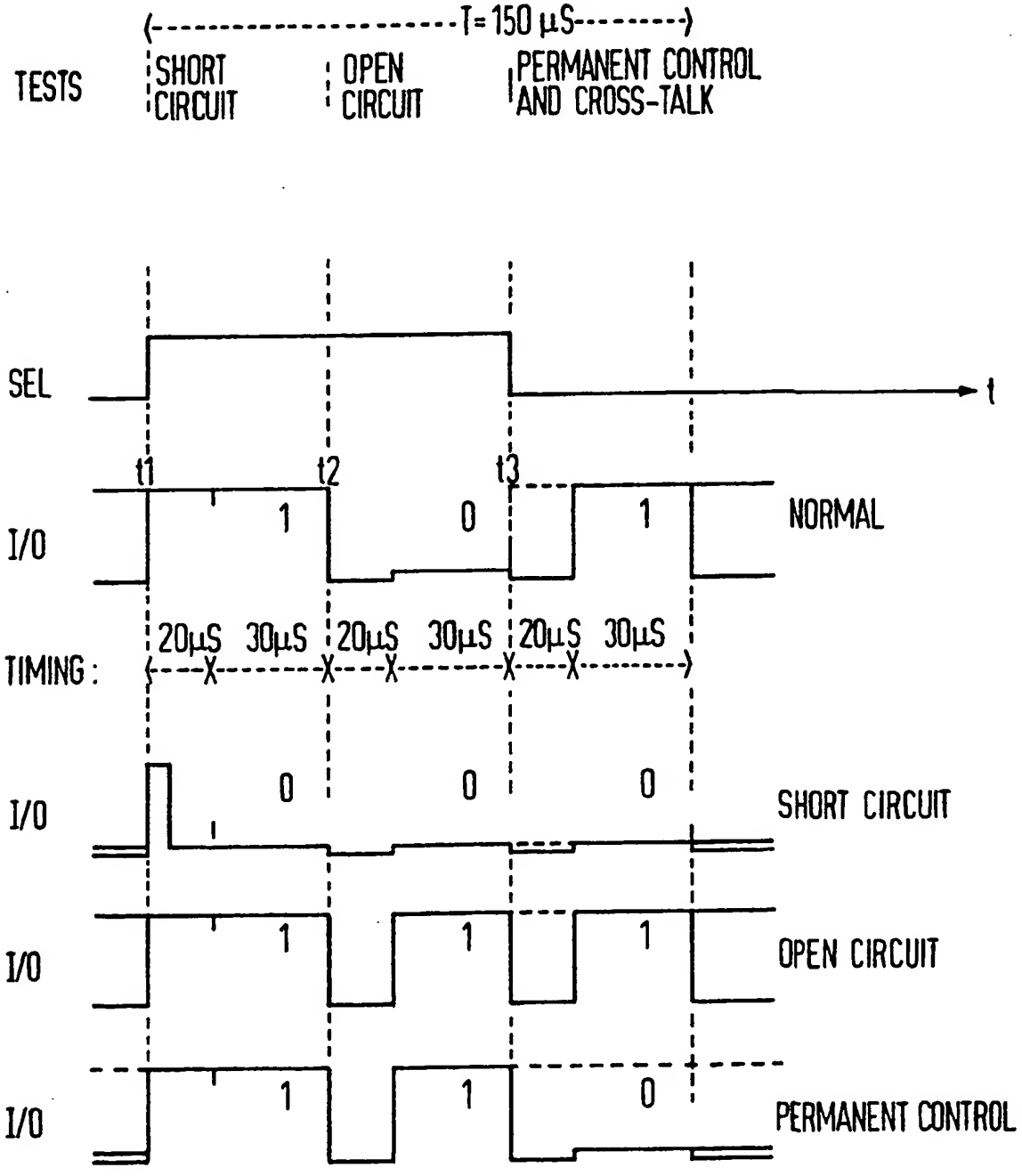

T = 150 µS
TESTS
SHORT CIRCUIT
OPEN CIRCUIT
PERMANENT CONTROL AND CROSS-TALK
SEL
t
t1
t2
t3
I/O
1
0
1
NORMAL
TIMING :
20µS 30µS 20µS 30µS 20µS 30µS
I/O
0
0
0
SHORT CIRCUIT
I/O
1
1
1
OPEN CIRCUIT
I/O
1
1
0
PERMANENT CONTROL

FIG 4

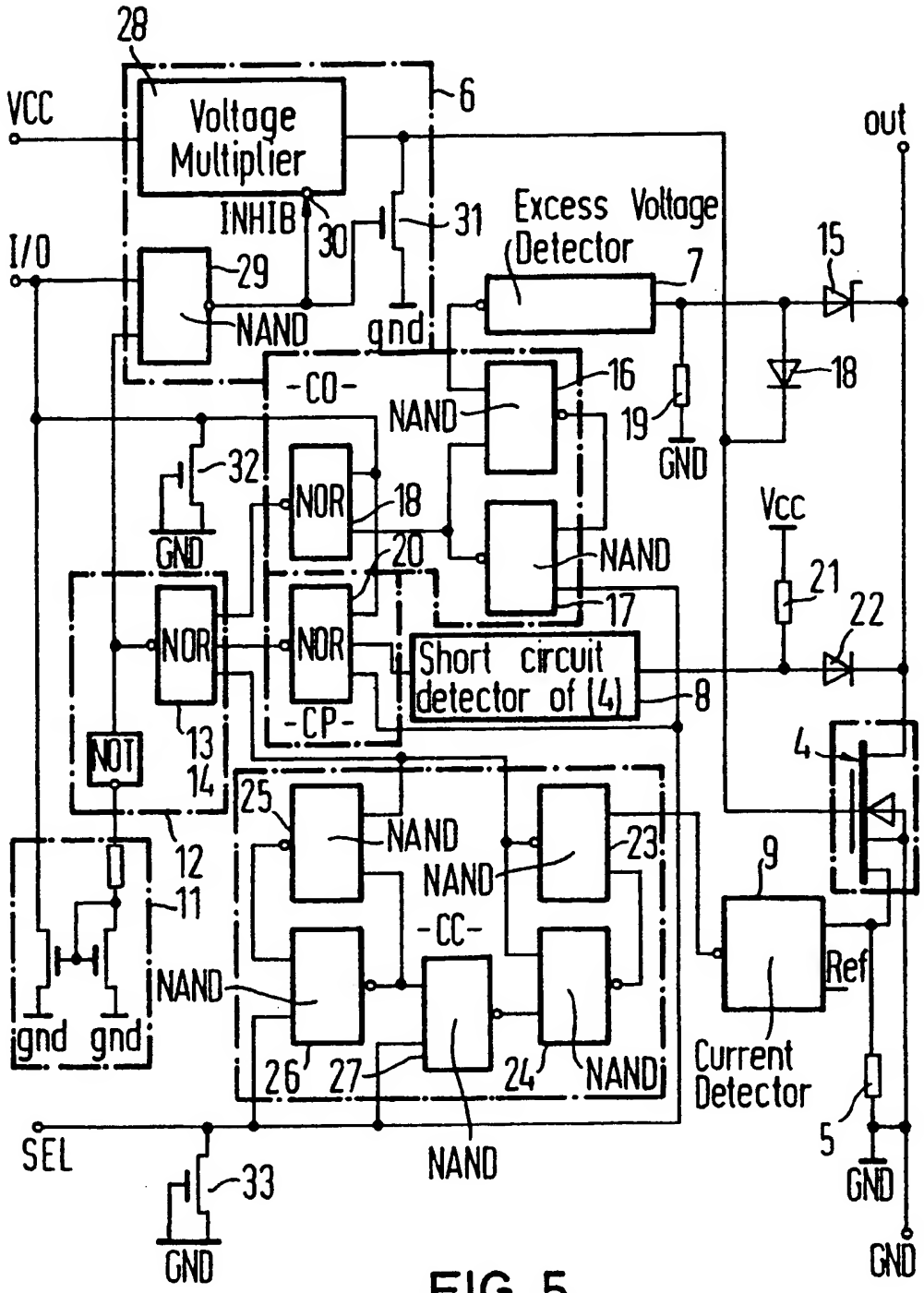

28
VCC
Voltage Multiplier
6
out
INHIB
30
31
Excess Voltage Detector
7
15
I/O
29
NAND
gnd
-CO-
16
NAND
19
18
GND
32
NOR
18
GND
20
NAND
Vcc
21
22
NOR
NOR
17
Short circuit detector of (4)
8
-CP-
13
NOT
14
4
25
NAND
23
12
NAND
9
11
-CC-
NAND
Ref
gnd gnd
26
27
24
NAND
Current Detector
SEL
NAND
5
33
GND
GND
GND

FIG 5

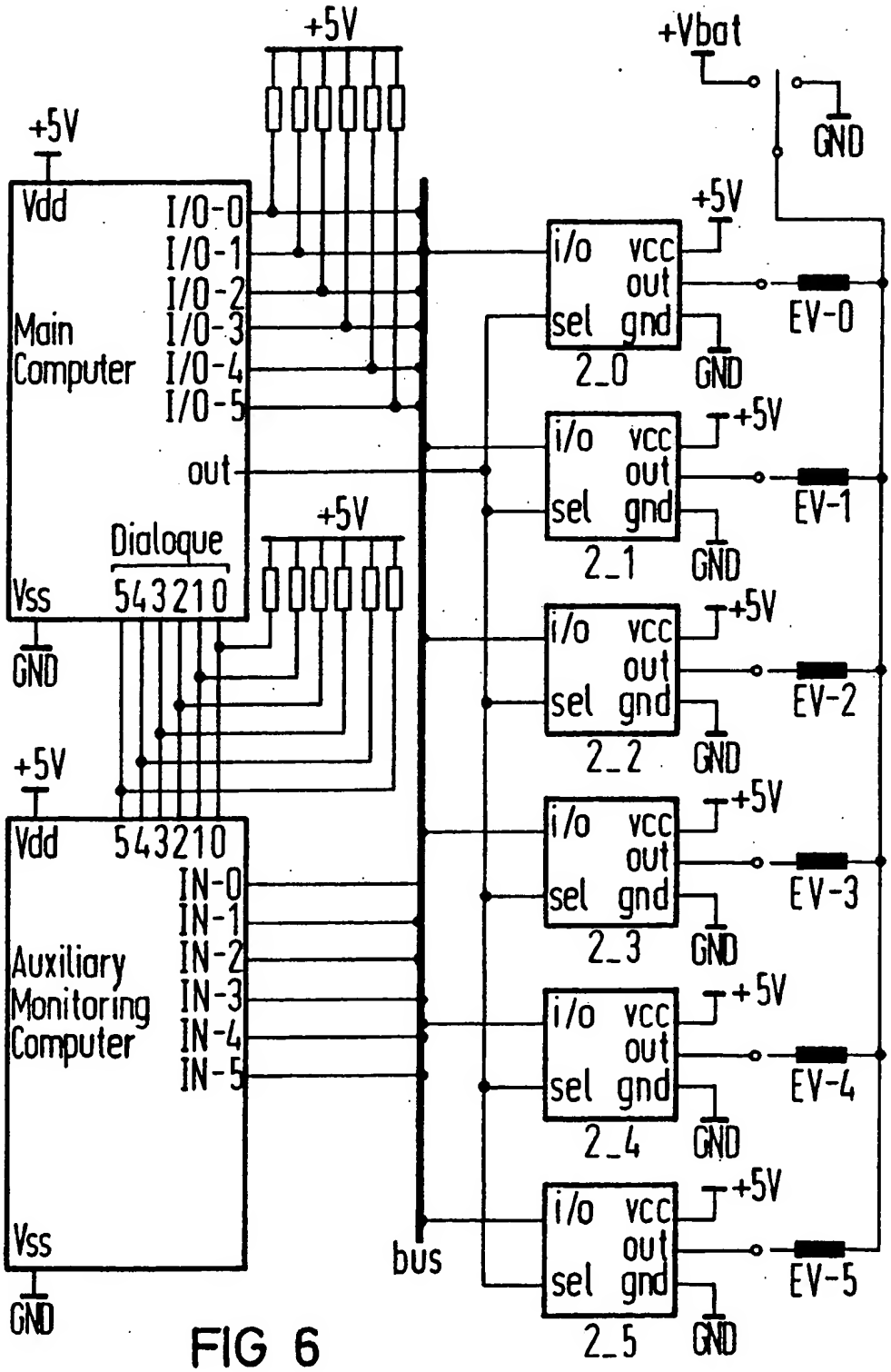

+5V
+5V
Vdd
I/O-0
I/O-1
I/O-2
Main
Computer
I/O-3
I/O-4
I/O-5
out
Dialoque
Vss
543210
GND
+5V
+5V
Vdd
543210
IN-0
IN-1
IN-2
Auxiliary
Monitoring
Computer
IN-3
IN-4
IN-5
Vss
GND
bus
+Vbat
GND
+5V
i/o vcc
out
sel gnd
2_0
GND
EV-0
+5V
i/o vcc
out
sel gnd
2_1
GND
EV-1
+5V
i/o vcc
out
sel gnd
2_2
GND
EV-2
+5V
i/o vcc
out
sel gnd
2_3
GND
EV-3
+5V
i/o vcc
out
sel gnd
2_4
GND
EV-4
+5V
i/o vcc
out
sel gnd
2_5
GND
EV-5

FIG 6

European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 90 11 7230

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
Y	US-A-4 799 126 (KRUSE et al.) * Abstract; column 3, line 55 - column 4, line 26; column 9, lines 41-46; figures 1,2 *	1-3	G 01 R 31/02 B 60 T 8/88 G 05 B 19/05 H 03 K 17/08 H 02 H 3/087
A		11,12	
Y	US-A-4 389 710 (RASMUSSEN) * Abstract; column 1, line 64 - column 2, line 8; column 4, lines 10-18; column 5, lines 39-62; figure 1 *	1-3	
A		9	
P,A	JP-A-1 227 611 (11-09-1989) * Abstract; page 2, lines 1-19; page 13, lines 350; figures 1,4,9,10 * & DE-A-3 906 886 (ALPS ELECTRIC)	1-3,5,6,9, 12	
A	EP-A-0 249 448 (MITSUBISHI) * Abstract; figure 1 *	1,2,5,6	
A	SIEMENS POWER ENGINEERING, vol. 5, no. 4, July/August 1983, pages 209-214; R. BECK et al.: "Simatic S5-110F programmable controller for safety-oriented control" * Page 211, left-hand column, last paragraph; figure 4 *	1,11,12	
A	EP-A-0 155 213 (MERLIN GERIN) * Abstract; page 6, line 5 - page 7, line 3; figures 1,2 *	1	
A	US-A-4 851 952 (COOK) * Abstract; column 2, lines 41-45; column 5, lines 46-58; figure 1 *	1,9	

TECHNICAL FIELDS SEARCHED (Int. Cl.5)
G 01 R B 60 T H 01 H H 02 H H 03 K G 05 B

The present search report has been drawn up for all claims

Place of search	Date of completion of search	Examiner
The Hague	14 December 90	SINAPIUS G.H.

CATEGORY OF CITED DOCUMENTS

X: particularly relevant if taken alone
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E: earlier patent document, but published on, or after the filing date
D: document cited in the application
L: document cited for other reasons

&: member of the same patent family, corresponding document